NP100N04NUJ

MOS FIELD EFFECT TRANSISTOR

R07DS0364EJ0100
Rev.1.00
Jun 13, 2011

Description

The NP100N04NUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
  — $R_{DS(on)}$ = 3.0 mΩ MAX. (V_{GS} = 10 V, I_D = 50 A)
- Low C_{iss}: C_{iss} = 5600 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- High current rating: $I_{D(DC)}$ = ±100 A
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing	Package
NP100N04NUJ–S18-AY *1	Pure Sn (Tin)	Tube 50 p/tube	TO-262 (MP-25SK) TYP. 1.8g

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±100	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±400	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	220	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *2	I_{AR}	60	A
Repetitive Avalanche Energy *2	E_{AR}	360	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.68	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W

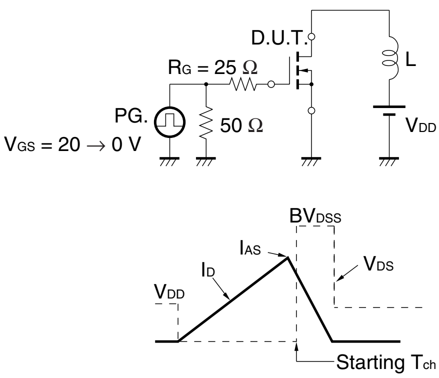
Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. $T_{ch(peak)}$ ≤ 150°C, R_G = 25 Ω

Electrical Characteristics (T_A = 25°C)

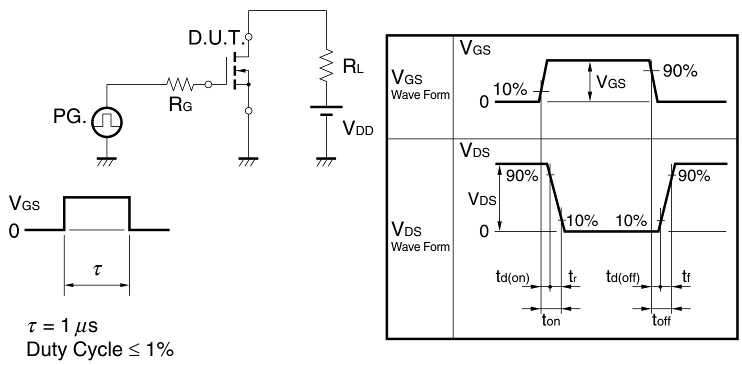
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1.0	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	$\| y_{fs} \|$	45	87		S	V_{DS} = 5 V, I_D = 50 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$		2.5	3.0	mΩ	V_{GS} = 10 V, I_D = 50 A
Input Capacitance	C_{iss}		5600	8400	pF	V_{DS} = 25 V,
Output Capacitance	C_{oss}		920	1380	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		340	620	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		25	60	ns	V_{DD} = 20 V, I_D = 50 A,
Rise Time	t_r		15	40	ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		93	190	ns	R_G = 0 Ω
Fall Time	t_f		13	40	ns	
Total Gate Charge	Q_G		110	170	nC	V_{DD} = 32 V,
Gate to Source Charge	Q_{GS}		22		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		32		nC	I_D = 100 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I_F = 100 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		55		ns	I_F = 100 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		77		nC	di/dt = 100 A/μs

Note: *1. Pulsed test

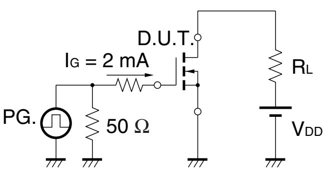
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

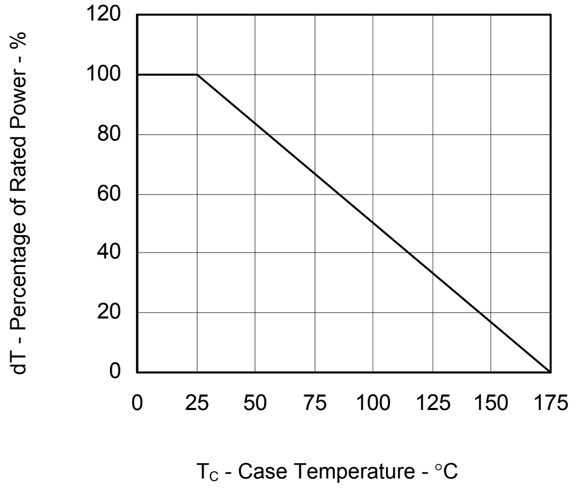


TEST CIRCUIT 3 GATE CHARGE

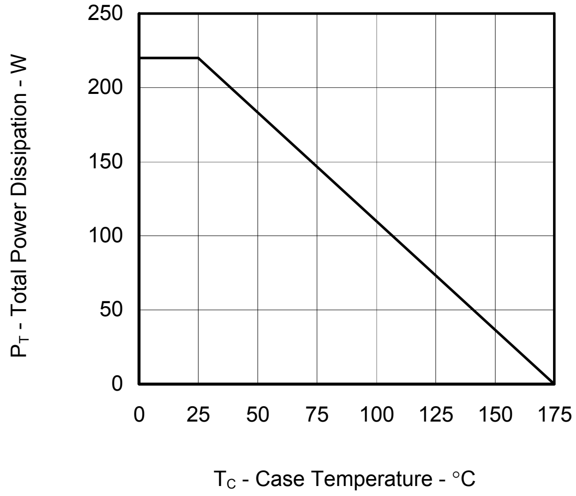


Typical Characteristics (T_A = 25°C)

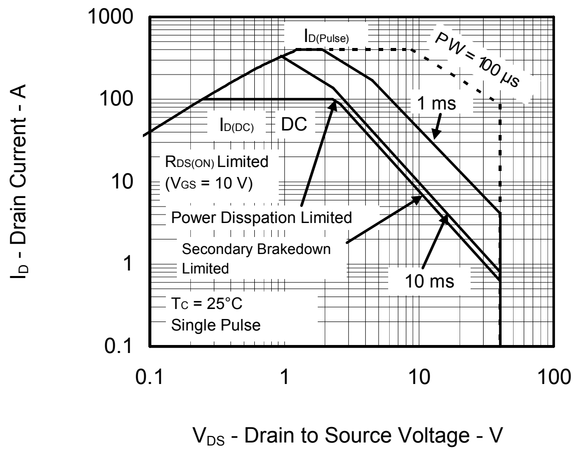
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



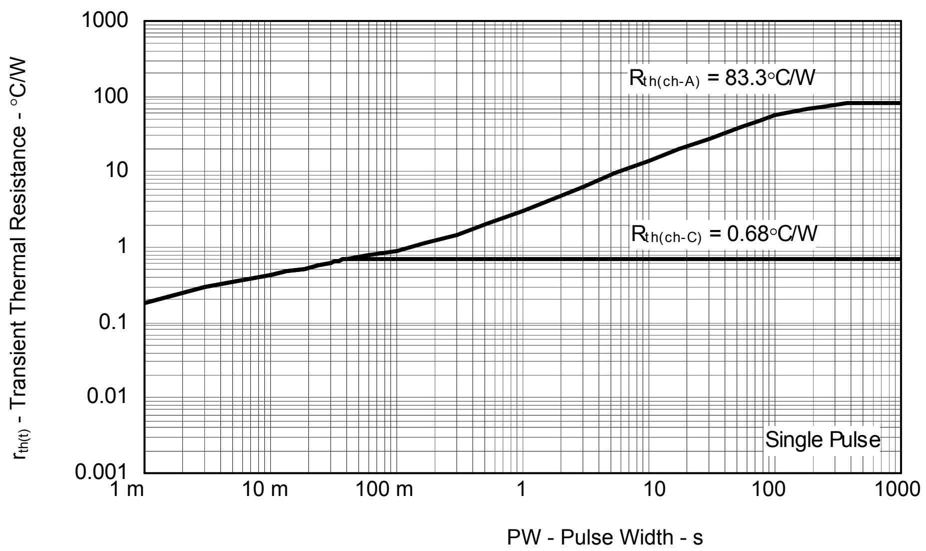
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



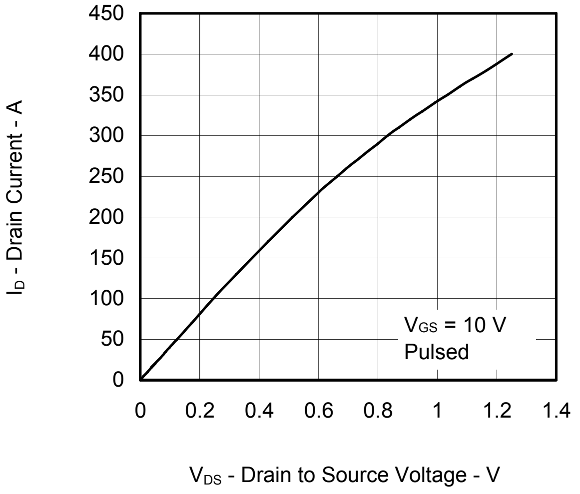
FORWARD BIAS SAFE OPERATING AREA



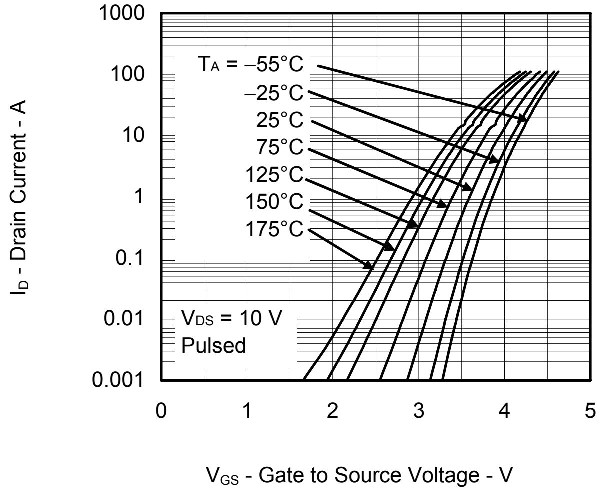
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



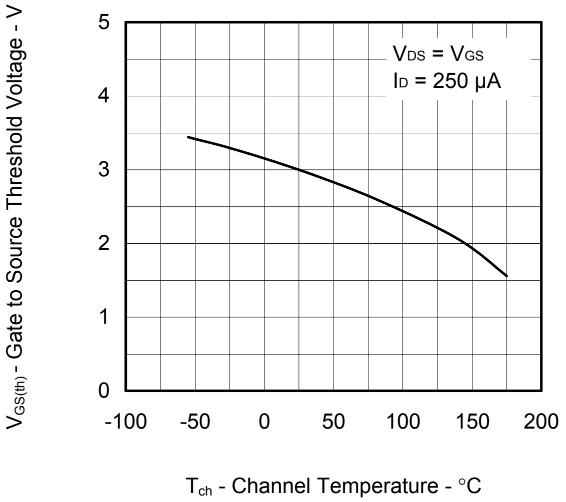
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



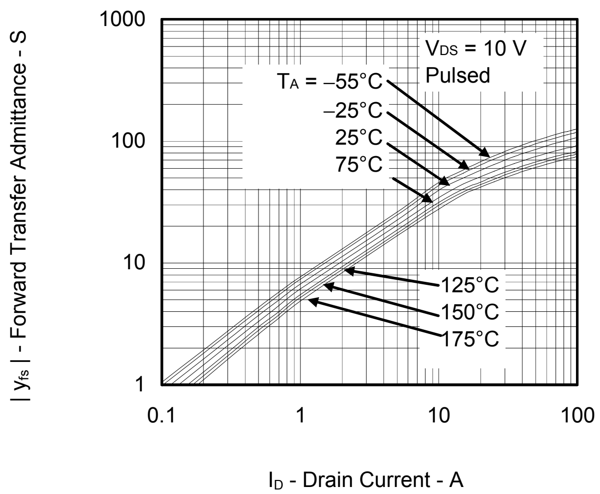
FORWARD TRANSFER CHARACTERISTICS



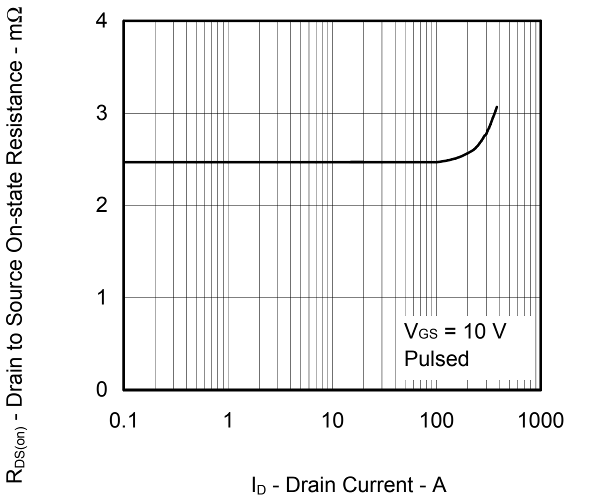
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATURE



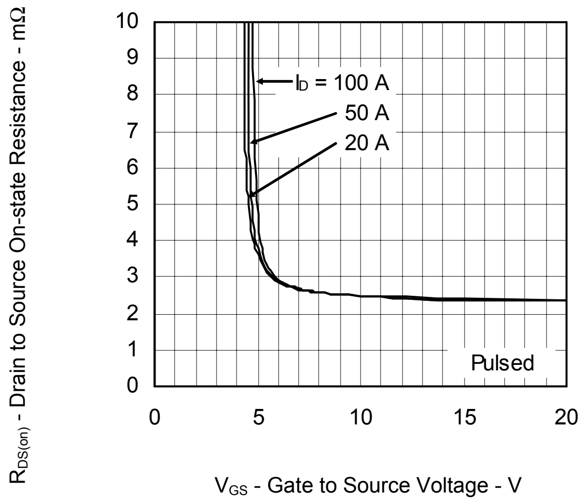
FORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENT



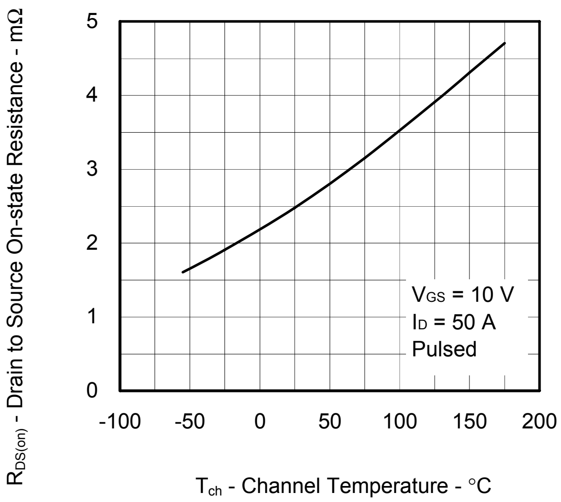
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



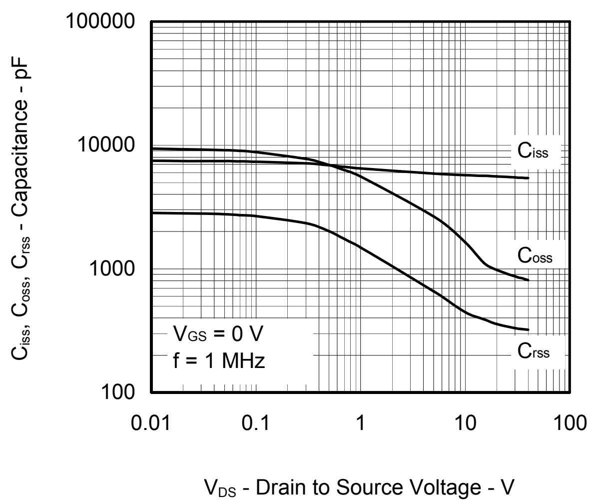
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



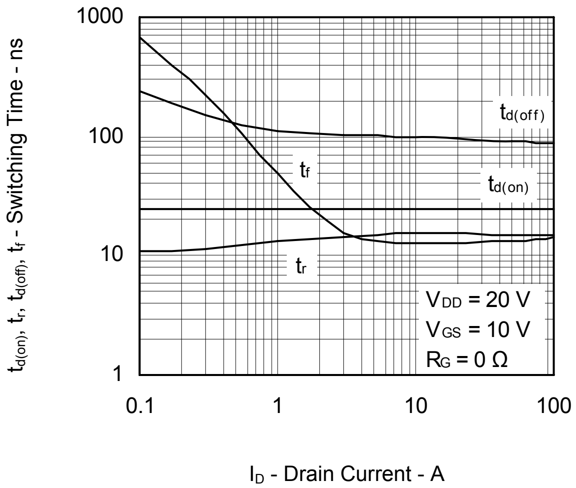
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



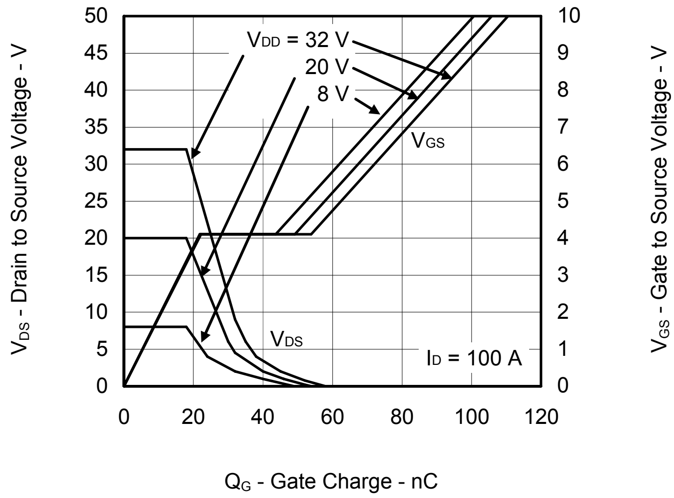
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



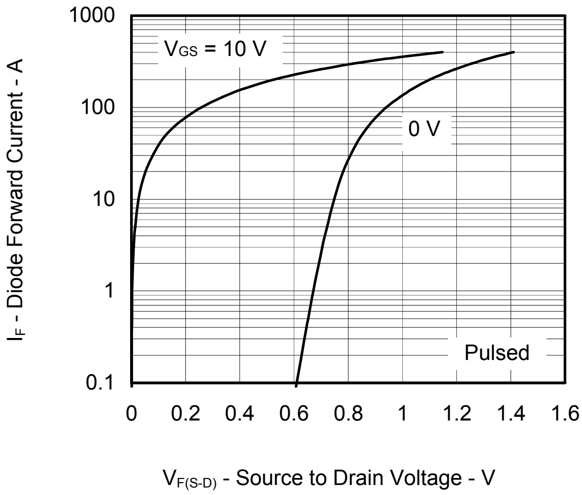
SWITCHING CHARACTERISTICS



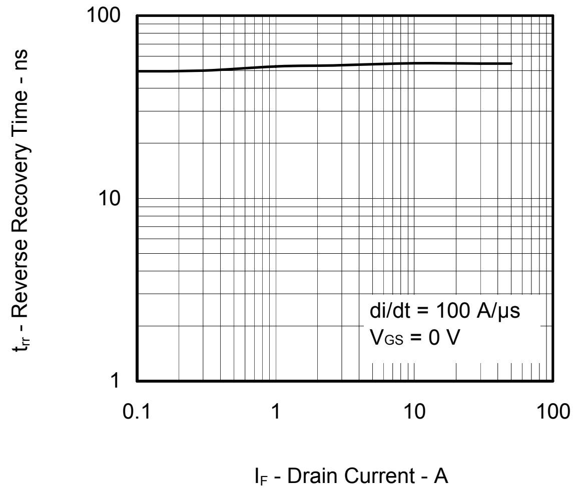
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

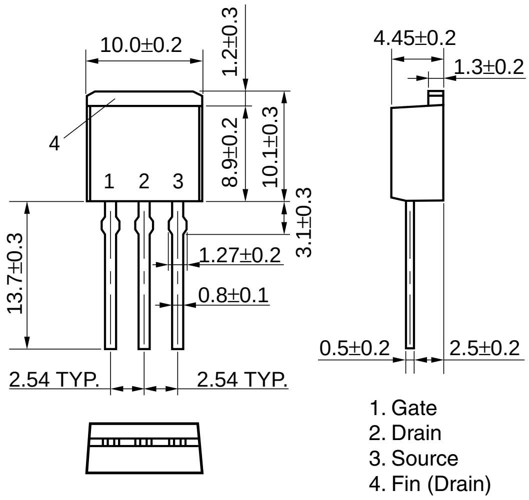


REVERSE RECOVERY TIME vs. DRAIN CURRENT

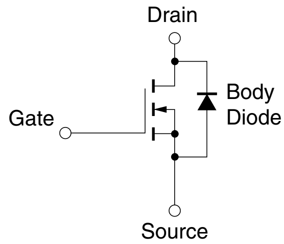


Package Drawings (Unit: mm)

TO-262 (MP-25SK)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP100N04NUJ Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun 13, 2011	–	First Edition Issued

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